ADVANCED COMPUTER ARCHITECTURE

Code: CS31127CS	Course Type: Elective	Semester: I
Evolution Scheme (TA-MSE-ESE): 20-30-100	Total Marks: 150	L-T-P (Credits): 3-0-0 (3)

Pre-Requisites: **NIL**

Course Objective: To develop a strong understanding of modern processor design, pipelining, and parallel execution techniques, along with memory hierarchy optimization and multicore architectures for high-performance scalable systems.

Course Outcomes: At the end of the course, the student will be able to

CO-1	Analyze processor performance and pipelined architectures, including hazard detection and resolution techniques.
CO-2	Apply instruction-level parallelism techniques such as dynamic scheduling, superscalar, and out-of-order execution.
CO-3	Design and evaluate memory hierarchy, including cache optimization and main memory systems.
CO-4	Evaluate multicore architectures and interconnection networks, including cache coherence and NoC design.

Course Articulation Matrix:

PO	PEO-1	PEO-2	PEO-3	PEO-4	PEO-5
CO-1	3	3	1	1	2
CO-2	3	3	2	1	3
CO-3	3	3	2	1	3
CO-4	3	3	2	2	3

1 - Slightly; 2 - Moderately; 3 – Substantially

Syllabus:

Unit-1: Pipeline Design and Performance Analysis

Review of computer architecture fundamentals, Performance metrics: CPI, speedup, execution time, Instruction pipelining concepts (RISC pipeline), Pipeline hazards: structural, data, control, Hazard detection and resolution techniques, Branch prediction methods and pipeline optimization.

Unit-2: Instruction-Level Parallelism and Advanced Processing

Instruction-Level Parallelism (ILP) concepts, Static vs dynamic scheduling, Tomasulo's algorithm, Speculative execution, Superscalar and out-of-order execution, Vector processors and GPU architecture.

Unit-3: Memory Hierarchy and Cache Optimization

Memory hierarchy design principles, Cache organization and mapping techniques, Replacement and write policies, Cache performance analysis, Cache optimization techniques, Main memory: DRAM organization and controllers.

Unit-4: Multicore Architectures and Interconnection Networks

Multicore and manycore architectures, Tiled Chip Multicore Processors (TCMP), Cache coherence basics, Network-on-Chip (NoC) concepts: Routing algorithms and router design. Emerging trends in computer architecture.

Learning Resources:

Text Books:

1. John L. Hennessy and David A. Patterson, Computer Architecture: A Quantitative Approach, 6th ed., Morgan Kaufmann, 2019.
2. John P. Shen and Mikko H. Lipasti, Modern Processor Design: Fundamentals of Superscalar Processors, Waveland Press, 2013.

Reference Books:

1. Kai Hwang, Advanced Computer Architecture: Parallelism, Scalability, Programmability, McGraw-Hill, 1993.
2. Michael J. Flynn and Wayne Luk, Computer System Design: System-on-Chip, Wiley, 2011.